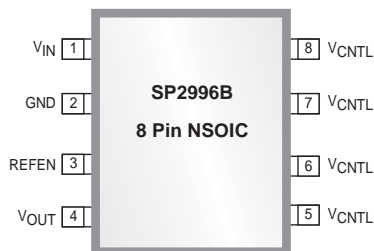


2 Amp DDR Bus Termination Regulator

FEATURES

- Capable of sourcing and sinking 2A Continuous current
- Supports both DDR1 (1.25V_{TT}) and DDR2 (0.9V_{TT}) requirements
- Low Output Voltage Offset, ± 20mV
- Thermal and Current Limit Protection
- Integrated Power MOSFETs
- Generates Termination for SSTL-2
- High Accuracy Output at Full Load
- Adjustable V_{OUT} by External Resistors
- Minimal External Components
- Available in 8 pin NSOIC package



Now Available in Lead Free Packaging

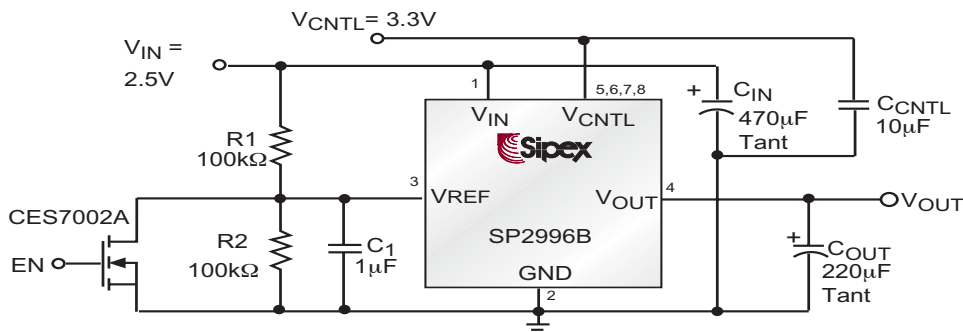
APPLICATIONS

- DDR Memory Termination
- Active Bus Termination
- Supply Splitter

DESCRIPTION

The SP2996B voltage regulator is designed to convert voltage supplies ranging from 1.6V to 6V into a desired output voltage which is adjusted by an external resistor divider. The regulator is capable of sourcing or sinking up to 2A of Continuous current while regulating an output voltage to within 20mV. The SP2996B provides an excellent voltage source for active termination schemes of high speed transmission lines such as those seen in high speed memory buses and distributed backplane designs when used in conjunction with series termination resistors. The voltage output of the regulator can be used as a termination voltage for DDR SDRAM, and it meets the JEDEC SSTL-2 and SSTL-3 specifications. Current limits in both sourcing and sinking mode, plus on-chip thermal shutdown make the circuit tolerant of output fault conditions.

TYPICAL APPLICATIONS CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage -0.4V to 7V
 Operating Temperature Range.....-40°C to +85°C
 Junction Temperature125°C
 Storage Temperature Range.....-65°C to +150°C

ELECTRICAL CHARACTERISTICS

$V_{IN} = 2.5V$, $V_{CTRL} = 3.3V$, $V_{REF} = 0.5V_{IN}$, $C_{OUT} = 10\mu F$ (Ceramic), $T_A = 25^\circ C$, unless otherwise specified. (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage Range (DDR 1/2) (Note 5)	V_{IN}	Keep V_{CTRL} V_{IN} on operation power on and power off sequences	1.6	2.5/1.8	-	V
	V_{CNTL}	$I_{OUT} = 0mA$	3.0	3.3	6	
Output Voltage	V_{OUT}	$I_{OUT} = 0mA$	V_{REF}			V
Output Offset Voltage	V_{OS}	No Load	-20	-	20	mV
Load Regulation (DDR 1/2)	V_{LOR}	$I_{OUT} = 0.1mA$ to +2A	-	10	25	mV
		$I_{OUT} = 0.1mA$ to -2A	-	10	25	
Quiescent Current	I_Q	$V_{REF} < 0.2V$, $V_{OUT} = OFF$	-	8	30	μA
Operating Current of V_{CNTL}	I_{CNTL}	No Load	-	3	10	mA
Bias Current of V_{REF}		$V_{REF} = 1.25V$	-	-	1	μA
Current Limit	I_{IL}	Note 4	2.2	3	4.5	A
Thermal Protection						
Thermal Shutdown Temperature (Note 5)	T_{SD}	3.3V V_{CNTL} 5V Guaranteed by design	125	150	-	$^\circ C$
Thermal Shutdown Hysteresis		Guaranteed by design	-	30	-	$^\circ C$
Shutdown Specifications						
Shutdown Threshold	$V_{TRIGGER}$	Output ON ($V_{REF} = ZeroV$ ---->1.25V)	0.8	-	-	V
Shutdown Threshold	$V_{TRIGGER}$	Output OFF ($V_{REF} = 1.25V$ ----> ZeroV)	-	-	0.2	
Thermal Resistance	θ_{JA}			160		$^\circ C/W$
	θ_{JC}			40		

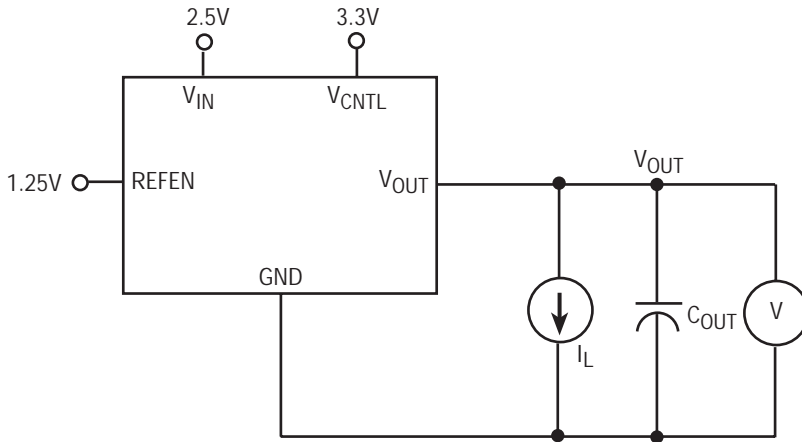
Note 1 . Specifications are tested for production at $T_A = 25^\circ C$. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2. V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REF} .

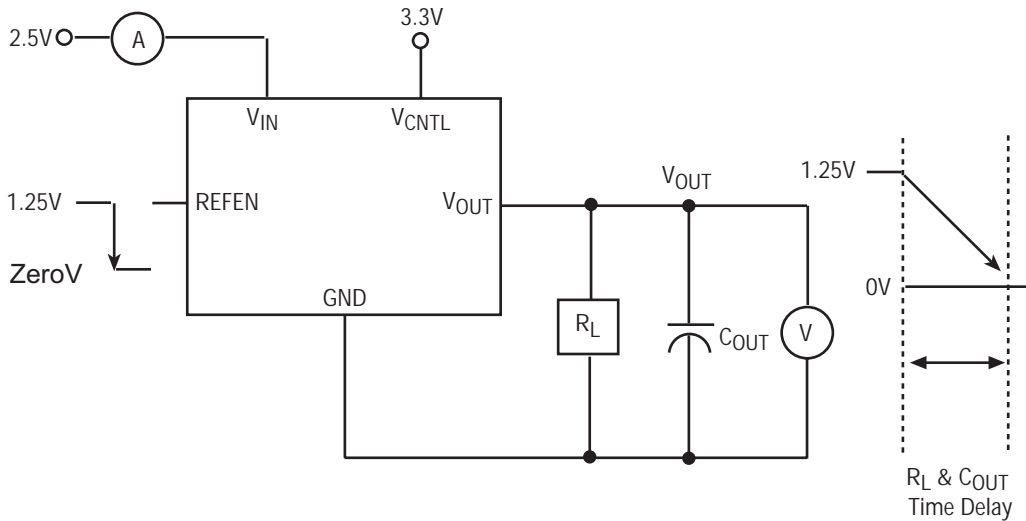
Note 3. Load regulation is measured at constant junction temperature, using pulse testing with a low ON time.

Note 4. Current limit is measured by pulsing a short time.

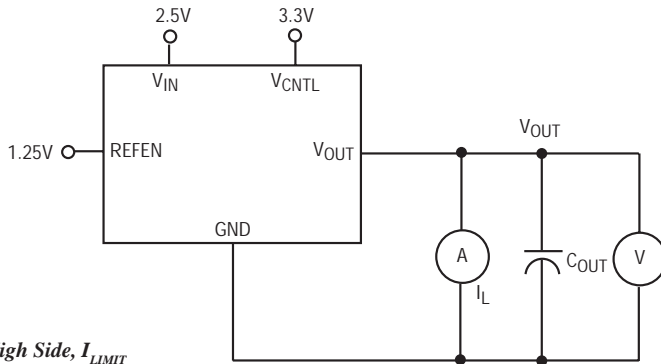
Note 5. In order to safely operate your system, V_{CTRL} must be $> V_{IN}$.



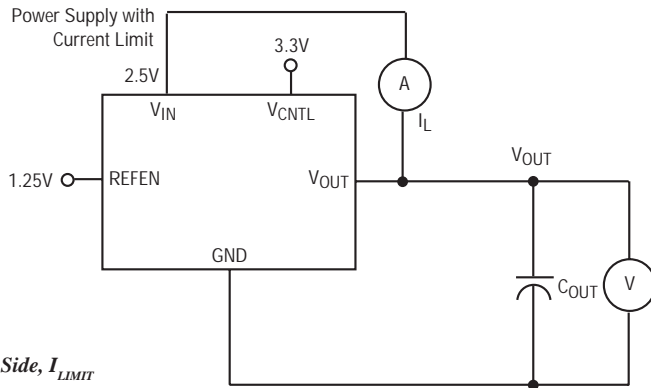
Testing Output Voltage Tolerance, ΔV_{LOAD}



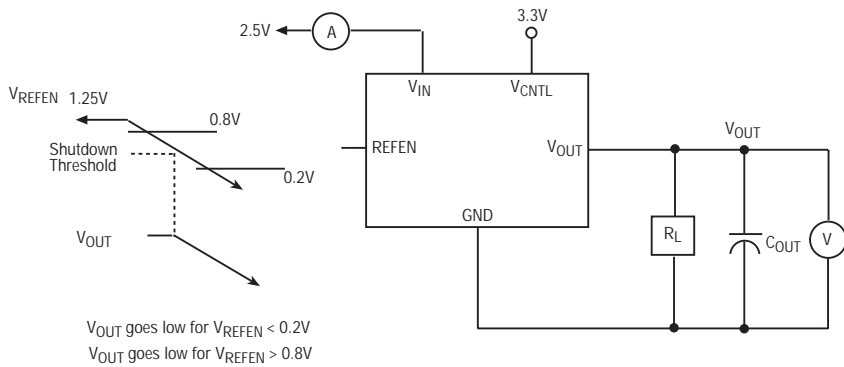
Testing Current in Shutdown Mode, I_{SHDN}



Testing Current Limit for High Side, I_{LIMIT}

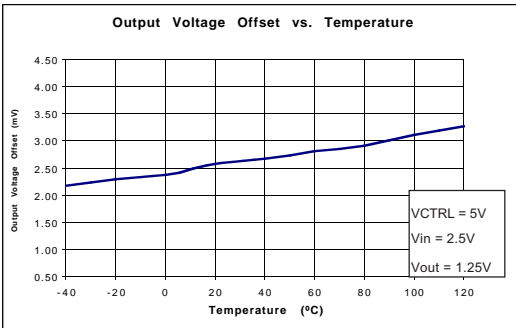
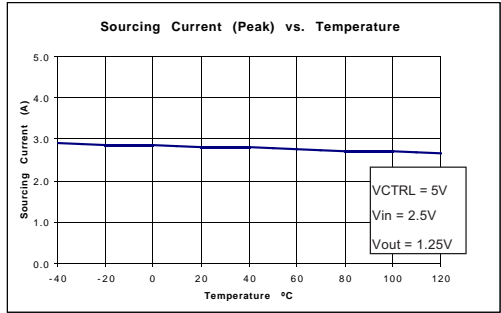
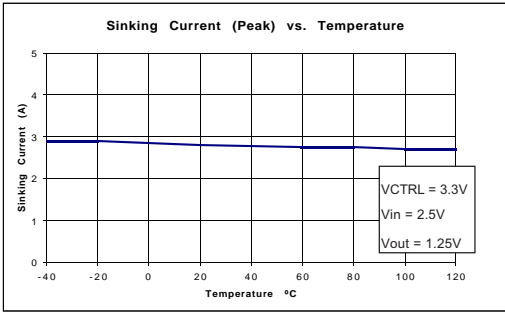
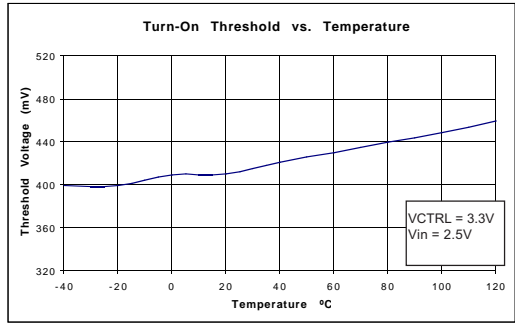
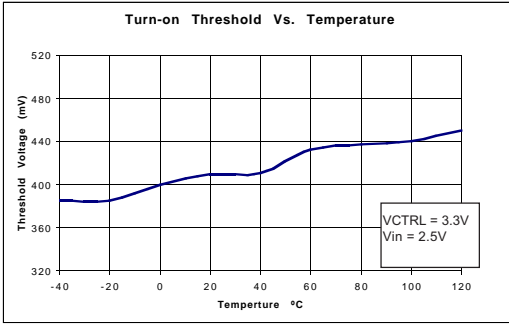


Testing Current Limit for Low Side, I_{LIMIT}

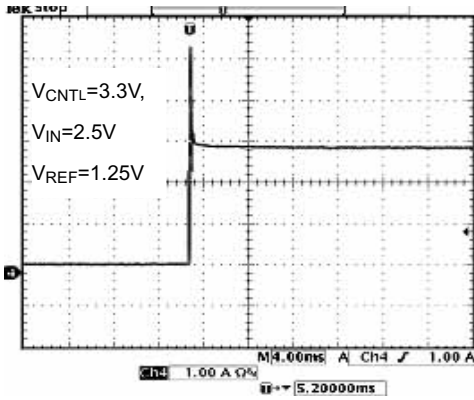


Testing REFEN Pin Shutdown Threshold, $V_{TRIGGER}$

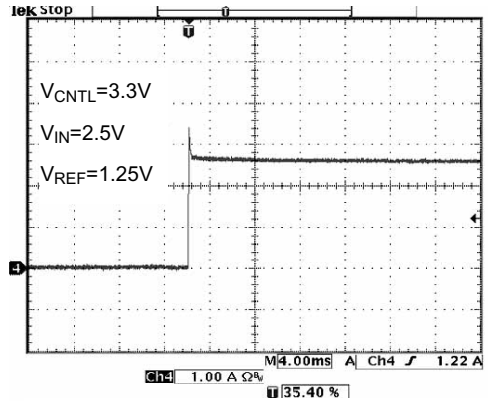
TYPICAL PERFORMANCE CHARACTERISTICS



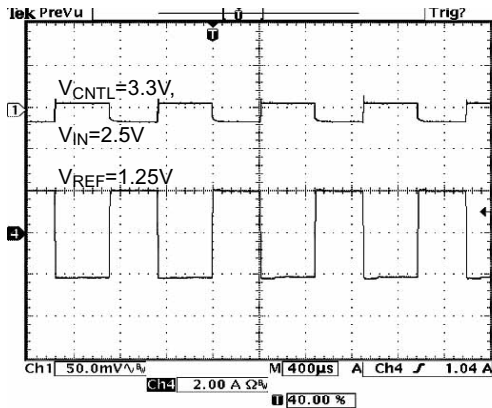
TYPICAL PERFORMANCE CHARACTERISTICS



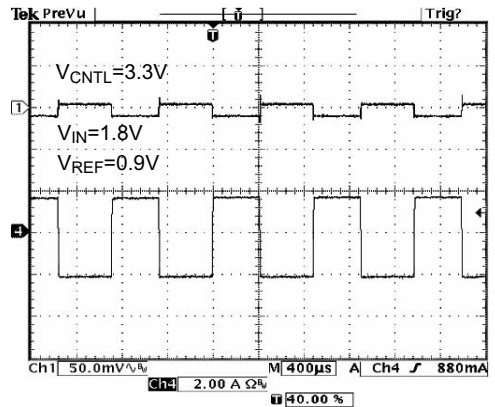
Output Short-Circuit (Sinking)



Output Short-Circuit (Sourcing)



Transient Response at $1.25V_{TT}/2A$



Transient Response at $0.9V_{TT}/2A$

Internal parasitic diode

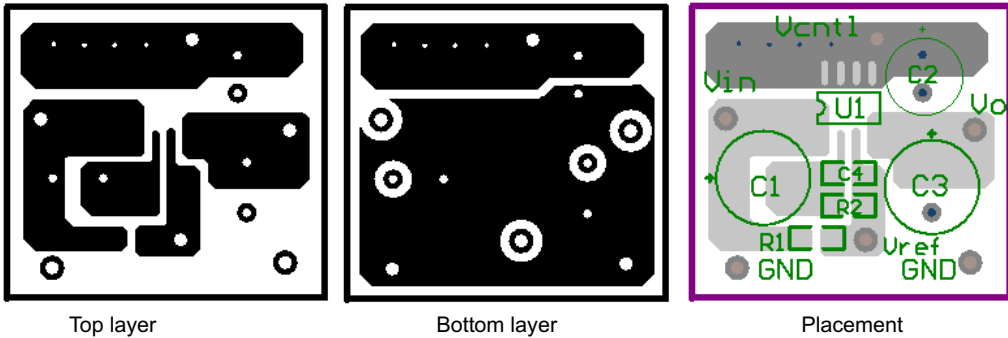
Avoid forward-biasing the internal parasitic diode, V_{OUT} to V_{CNTL} , and V_{OUT} to V_{IN} . Positive voltage should not be applied to the output if V_{IN} and V_{CNTL} are not present.

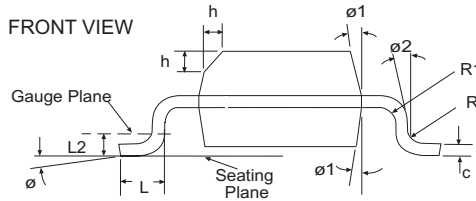
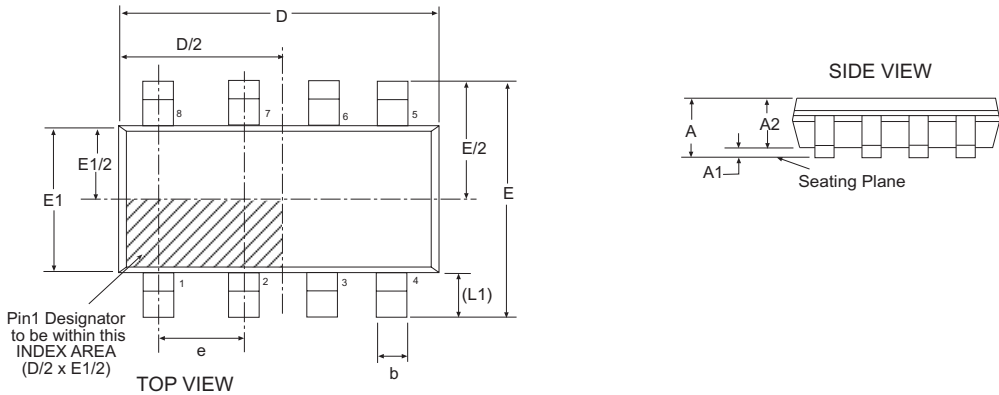
Considerations for designing, resistance of voltage divider

When the reference voltage is programmed below 0.2V the pull-down capability of the internal NMOS transistor is limited. It is recommended to place a filter capacitor from V_{RE} to ground in order to reduce sensitivity to noise and improve power up characteristics (soft start).

Layout Considerations

The SP2996B is offered in the NSOIC-8 package, resulting in attention needing to be paid to dissipating heat effectively when it operates in high current. In order to prevent maximum junction temperature from being exceeded, suitable copper area is necessary. The large copper area at V_{CNTL} pins is available, and by taking advantage of this, much heat dissipation is attained. Use vias to direct heat into the bottom layer as the layout examples show below. All capacitors should be placed as close as possible to relative pins.





8 Pin NSOIC		JEDEC MS-012		Variation AA		
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	-	1.75	0.053	-	0.069
A1	0.10	-	0.25	0.004	-	0.010
A2	1.25	-	1.65	0.049	-	0.065
b	0.31	-	0.51	0.012	-	0.020
c	0.17	-	0.25	0.007	-	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	-	0.50	0.010	-	0.020
L	0.40	-	1.27	0.016	-	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
theta	0°	-	8°	0°	-	8°
theta1	5°	-	15°	5°	-	15°
theta2	0°	-	-	0°	-	-
D	4.90 BSC			0.193 BSC		
SIPEX Pkg Signoff Date/Rev:				JL Aug16-05 / Rev A		

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SP2996BEN	-40°C to 85°C.....	8 Lead NSOIC
SP2996BEN/TR	-40°C to 85°C.....	8 Lead NSOIC

Available in lead free packaging. To order add "-L" suffix to part number.

Example: SP2996BEN/TR = standard; SP2996BEN-L/TR = lead free.

/TR = Tape and Reel

Pack quantity is 2,500 for NSOIC.