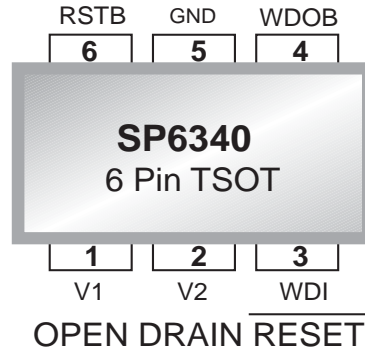


## Dual $\mu$ Power Supervisory Circuit with Watchdog

### FEATURES

- Low operating voltage of 1.6V
- Low operating current of 20 $\mu$ A typical
- Monitors 2 supplies simultaneously
- Reset asserted down to 0.9V
- 2% accuracy over temperature range
- Open Drain (OD) or CMOS RSTB output
- 4 Reset Timeout Periods  
50ms, 100ms, 200ms, and 400ms
- Watch Dog Timer Function
- Independent Open Drain Watchdog Output
- TSOT-6 package

*Available in Lead Free Packaging*

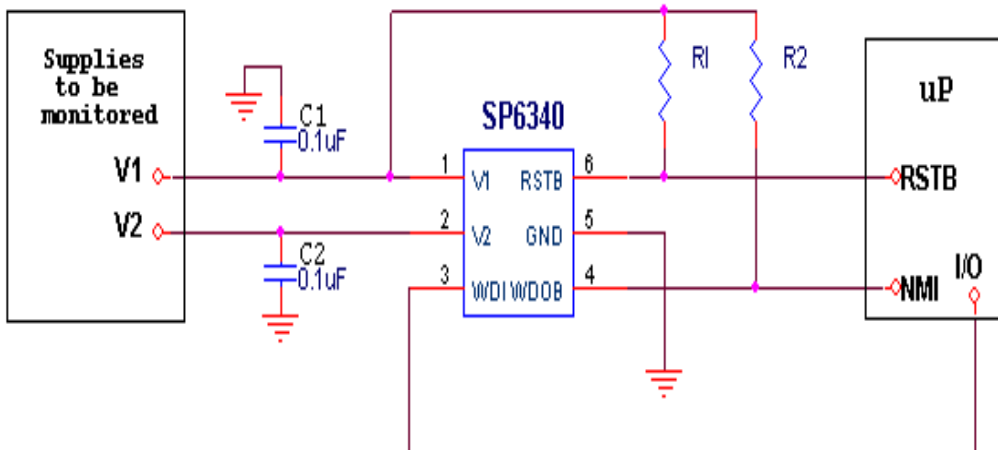


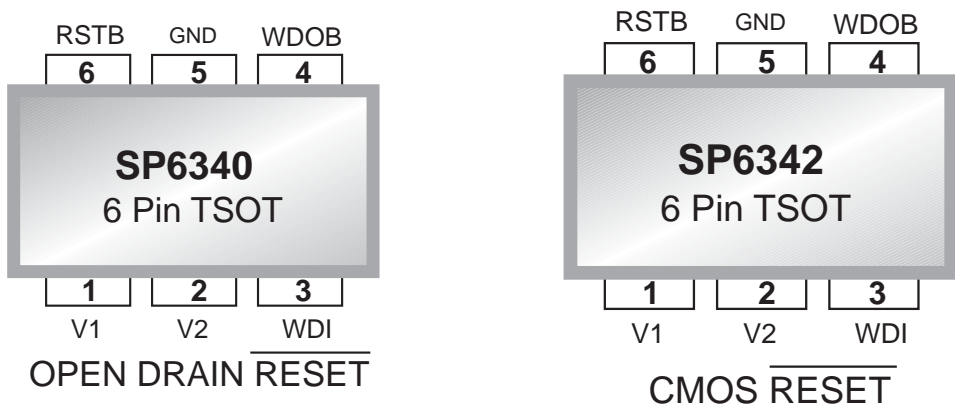
**SEE PAGE 2 FOR OTHER AVAILABLE PINOUTS**

### DESCRIPTION

SP6340 and SP6342 Dual  $\mu$ Power Supervisory Circuit Family is a family of microprocessor reset supervisory circuits with multiple reset voltages. The family provides low voltage monitoring ability for up to two supplies with two precision factory-set thresholds. These circuits perform a single function: if any of the input supply voltages drops below its associated threshold, reset outputs are asserted. Products in the family offer watchdog functionalities. SP6340 and SP6342 are packaged in a 6-pin TSOT package. All devices are fully specified over -40°C to +85°C temperature range.

### TYPICAL APPLICATION CIRCUIT





PART NUMBER	V1	V2	Reset	WatchDog Input	WatchDog Output BAR
SP6340			OD Active Low		OD Active Low
SP6342			CMOS Active Low		CMOS Active Low

Feature and Pinout Diagram

**ABSOLUTE MAXIMUM RATINGS**

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

- Terminal Voltage (with respect to GND)  
V1, V2..... -0.3 to +6V
- Open-Drain RSTB,  
WDOB.....-0.3 to +6V
- CMOS RSTB,  
WDOB..... -0.3 to (V1+0.3V)

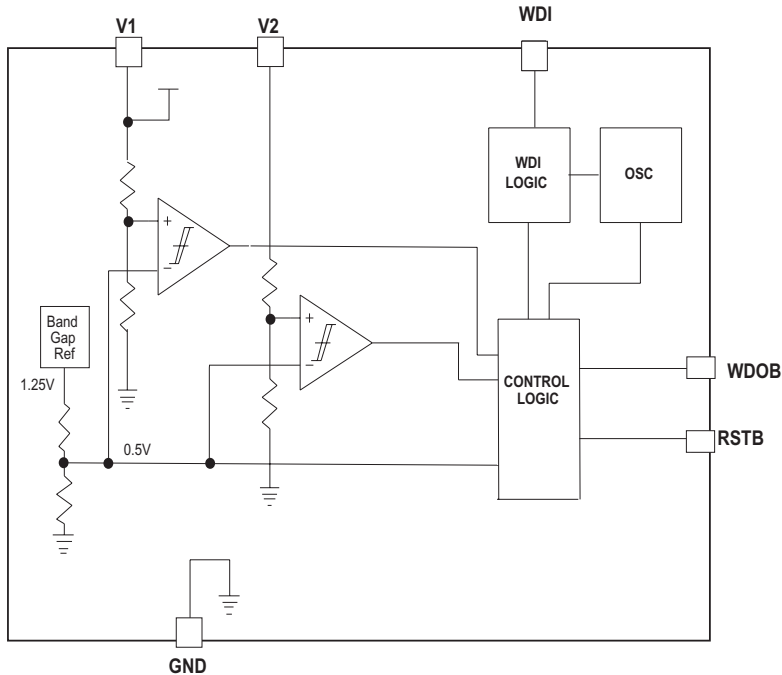
- Input Current/Output  
Current.....20mA
- WDI.....-0.3 to (V1+0.3V)
- Operating Temperature  
Range.....-40°C to +85°C
- Storage Temperature  
Range.....-65°C to 150°C
- Thermal Resistance  $\theta_{JA}$ .....134°C/W

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V1 = 1.6V to 5.5V; TA = -40°C to +85°C; unless otherwise noted. Typical values are at TA = +25°C					
Operating Voltage Range	0.9		5.5	V	TA = -40°C to +85°C
Supply Current		20	30	uA	V1 < 5.5V, V2 < 3.60V, all I/O pins open
		15	25		V1 < 3.6V, V2 < 2.75V, all I/O pins open
V1 Reset Threshold	4.532	4.625	4.718	V	Z (valid for V1 falling)
	4.287	4.375	4.463		Y (valid for V1 falling)
	3.013	3.075	3.137		X (valid for V1 falling)
	2.866	2.925	2.984		W (valid for V1 falling)
	2.572	2.625	2.678		V (valid for V1 falling)
	2.273	2.320	2.367		U (valid for V1 falling)
	2.146	2.190	2.234		T (valid for V1 falling)
	1.636	1.670	1.704		S (valid for V1 falling)
	1.548	1.580	1.612		R (valid for V1 falling)
V2 Reset Threshold	2.266	2.313	2.360	V	J (valid for V2 falling)
	2.144	2.188	2.232		I (valid for V2 falling)
	1.631	1.665	1.698		H (valid for V2 falling)
	1.543	1.575	1.607		G (valid for V2 falling)
	1.360	1.388	1.416		F (valid for V2 falling)
	1.286	1.313	1.340		E (valid for V2 falling)
	1.087	1.110	1.133		D (valid for V2 falling)
	1.029	1.050	1.071		C (valid for V2 falling)
	0.816	0.833	0.850		B (valid for V2 falling)
0.772	0.788	0.804	A (valid for V2 falling)		
Threshold 1 Tempco		0.06		mV/°C	
Threshold 2 Tempco		0.04		mV/°C	
Threshold 1 Hysteresis		0.65		%	reference to Vth1 typical
Threshold 2 Hysteresis		0.5		%	reference to Vth2 typical
V1 to RST/RSTB Delay		50		us	V1 = Vth1 to (Vth1-0.1V), Vth1 = 3.075
V2 to RST/RSTB Delay		50		us	V2 = Vth2 to (Vth2-0.1V), Vth2 = 1.575
Reset Timeout Period (T1)	37	50	63	ms	TOPT-1
Reset Timeout Period (T2)	74	100	126	ms	TOPT-2
Reset Timeout Period (T3)	148	200	252	ms	TOPT-3
Reset Timeout Period (T4)	296	400	504	ms	TOPT-4

**ELECTRICAL CHARACTERISTICS**  
**(CONTINUED)**

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V1 = 1.6V to 5.5V; T <sub>A</sub> = -40°C to +85°C; unless otherwise noted. Typical values are at T <sub>A</sub> = +25°C					
<b>WDI - WATCHDOG INPUT</b>					
Watchdog Timeout Period	1.2	1.6	2	sec	
WDI Pulse Width	0.1			us	
WDI Input Threshold			0.2*V1	V	V <sub>il</sub>
WDI Input Threshold	0.8*V1			V	V <sub>ih</sub>
WDI Input Current	-500		500	nA	WDI = 0.0V or V1
<b>RESET / WATCHDOG OUTPUTS</b>			<b>RSTB / WDOB</b>		
RSTB (CMOS or OD)			0.4	V	V1 = V <sub>th1</sub> - 0.1V, I <sub>sink</sub> = 1mA, output asserted
RSTB (CMOS)	0.8*V1			V	V1 = V <sub>th1</sub> + 0.1V, I <sub>source</sub> = 1mA, output not asserted
WDOB (CMOS or OD)			0.4	V	WDI = 0.0V or V1, V1 > V <sub>th1</sub> , V2 > V <sub>th2</sub> , I <sub>sink</sub> = 1mA, WDOB output asserted
WDOB (CMOS)	0.8*V1			V	V1 > V <sub>th1</sub> , V2 > V <sub>th2</sub> , WDOB not asserted, I <sub>source</sub> = 1mA
RSTB / WDOB Output OD Leakage Current		2		nA	T <sub>A</sub> = +25°C

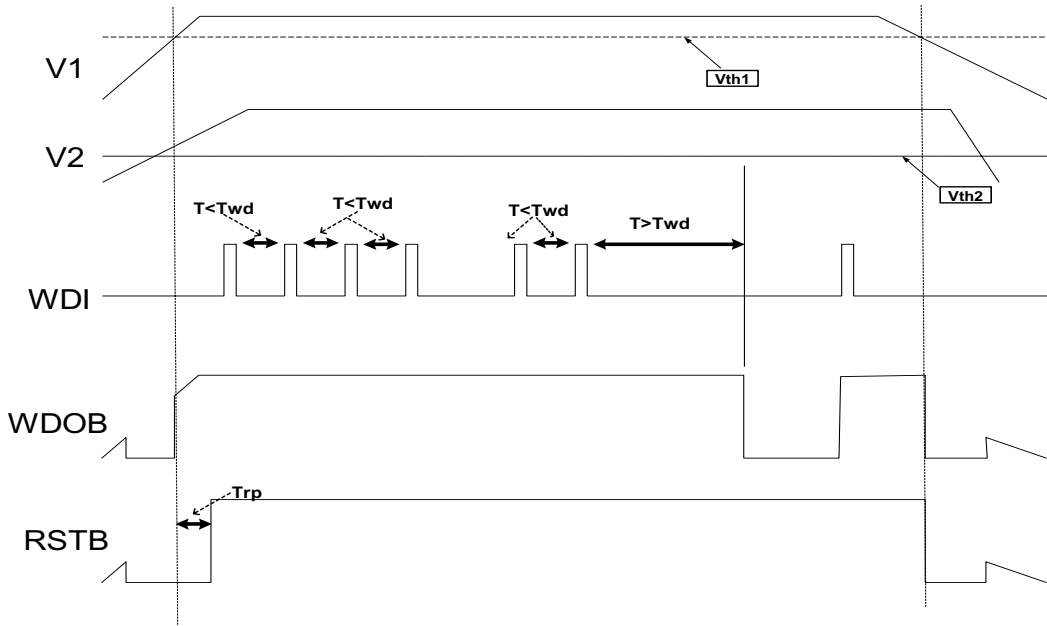
Pin #	Name	Description
1	V1	First supply voltage input. Also powers internal circuitry. Trip threshold voltage internally set.
2	V2	Second supply voltage input. Trip threshold voltage internally set.
3	WDI	Watch-Dog Input pin. When no transition is detected at the WDI pin for the duration of WDI timeout period, reset is asserted. WDOB remains at "LOW" logic level after watchdog timeout period is expired and it remains "LOW" until WDI makes a transition. RST/RSTB output is not affected by the watchdog functionality in the parts with separate WDOB output. The watchdog timer clears whenever the reset is asserted or a transition is observed at WDI pin.
4	WDOB	Watch Dog Output. Open-Drain or CMOS, active LOW. If WDI remains at "HIGH" or "LOW" logic level for longer than the watchdog timeout period, the internal watchdog timer overflows and WDOB is asserted. WDOB does not de-assert until the watchdog is cleared via transition at the WDI pin. Another scenario for WDOB to assert is when the reset output is asserted due to an under-voltage V1 or V2 condition. WDO de-asserts without a reset timeout period. Floating WDI will not disable watchdog timer in devices with dedicated WDOB output. Open-drain WDOB outputs require an external pull-up resistor. CMOS outputs are referenced to V1.
5	GND	Common ground reference pin.
6	RSTB	Reset output. Open-Drain or CMOS, active high or low. Reset is asserted when any of the supply inputs is below its trip threshold. It stays asserted for 200 ms (typical / default) after the last supply input traverses its trip threshold. Reset is guaranteed to be in the correct state for V1>0.9V. RSTB asserts when V1 or V2 drop below their corresponding reset thresholds. RSTB remains asserted for the reset timeout period after V1 and V2 exceed their corresponding reset thresholds. Open-drain outputs require an external pull-up resistor. CMOS outputs are referenced to V1.



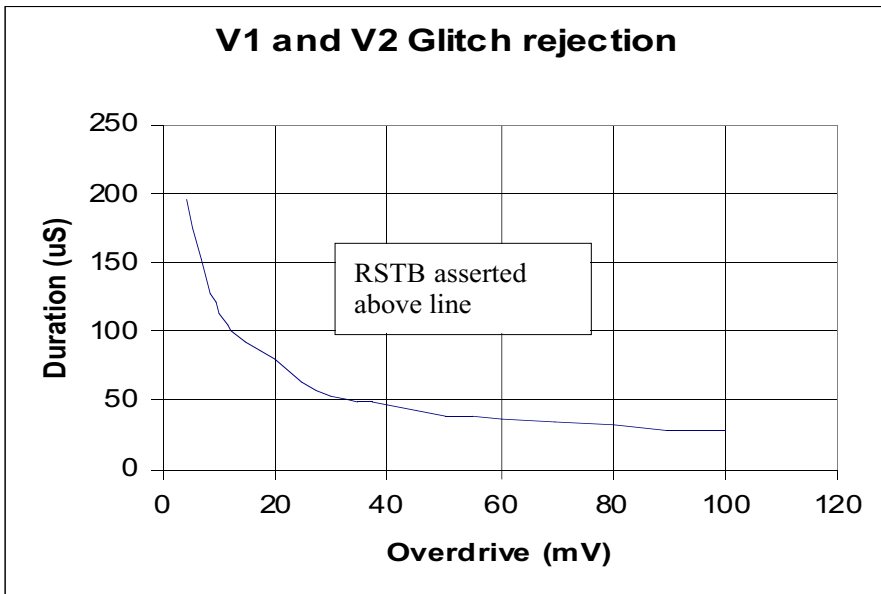
*Block Diagram*

The SP6340-SP6342 family includes a low-voltage precision bandgap reference, two precision comparators, an oscillator, a digital counter chain, a logic control block, trimmed resistor divider chains and additional supporting circuitry. The family is designed

to supervise 2 independent supply voltages. V1 and V2 supply inputs have their resistor dividers on the chip. Their trip thresholds are factory trimmed. The parts are furnished with watchdog input and output functionalities.

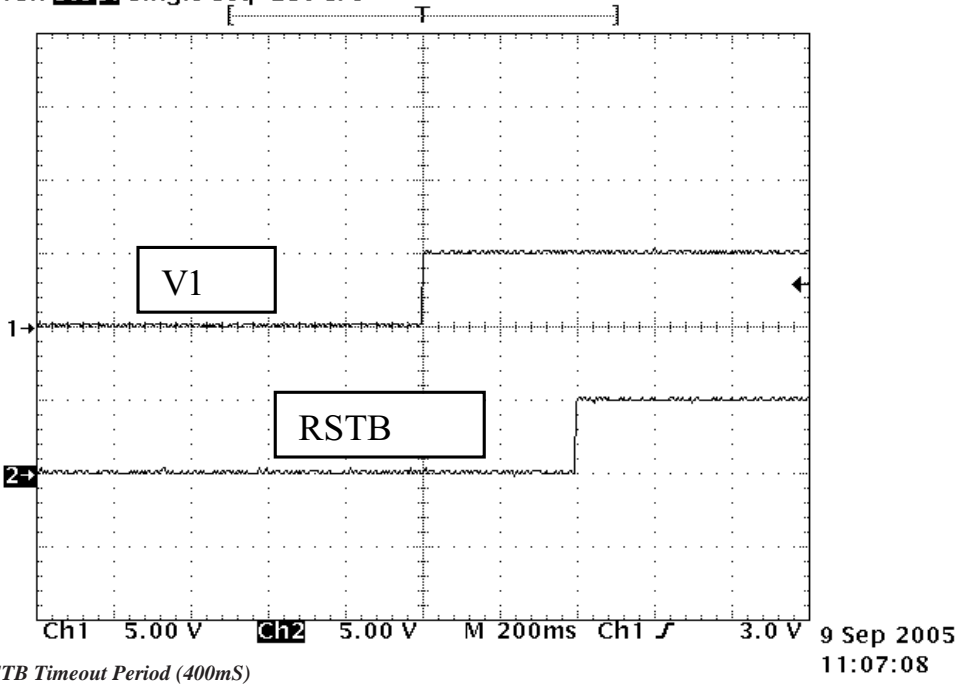


Timing Diagram for SP6340, SP6342

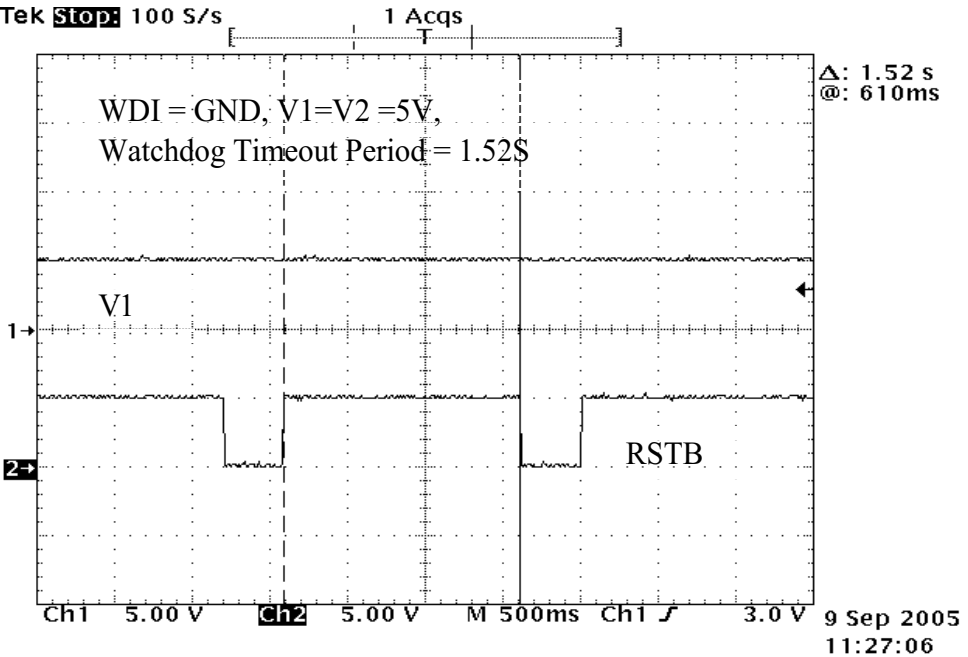


V1 and V2 Glitch Rejection

Tek **Stop:** Single Seq 250 S/s

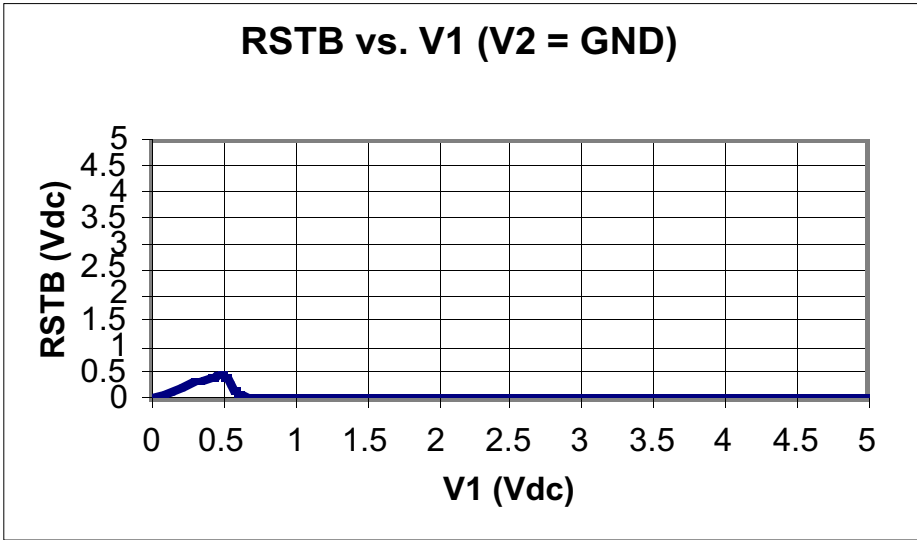


Tek **Stop:** 100 S/s

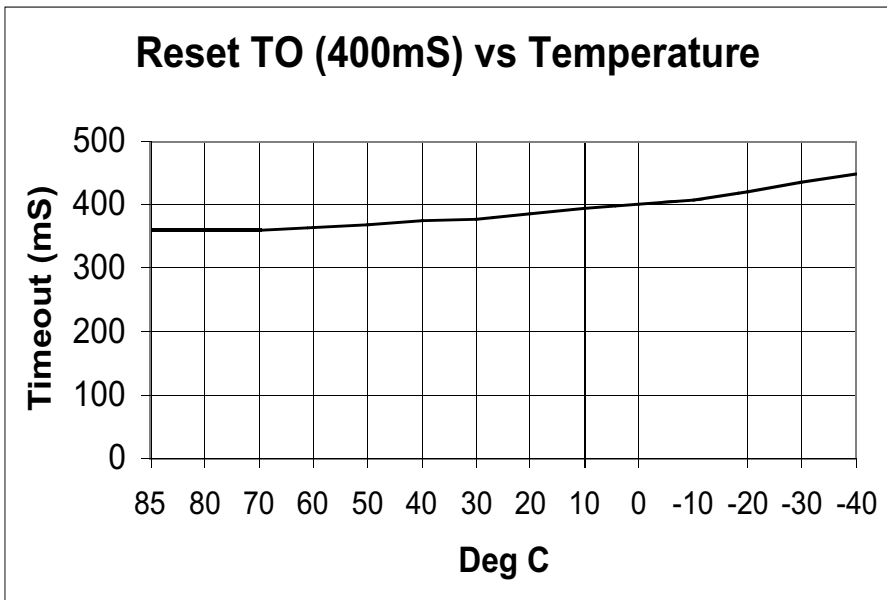


*SP6340 Watchdog Timeout Period*





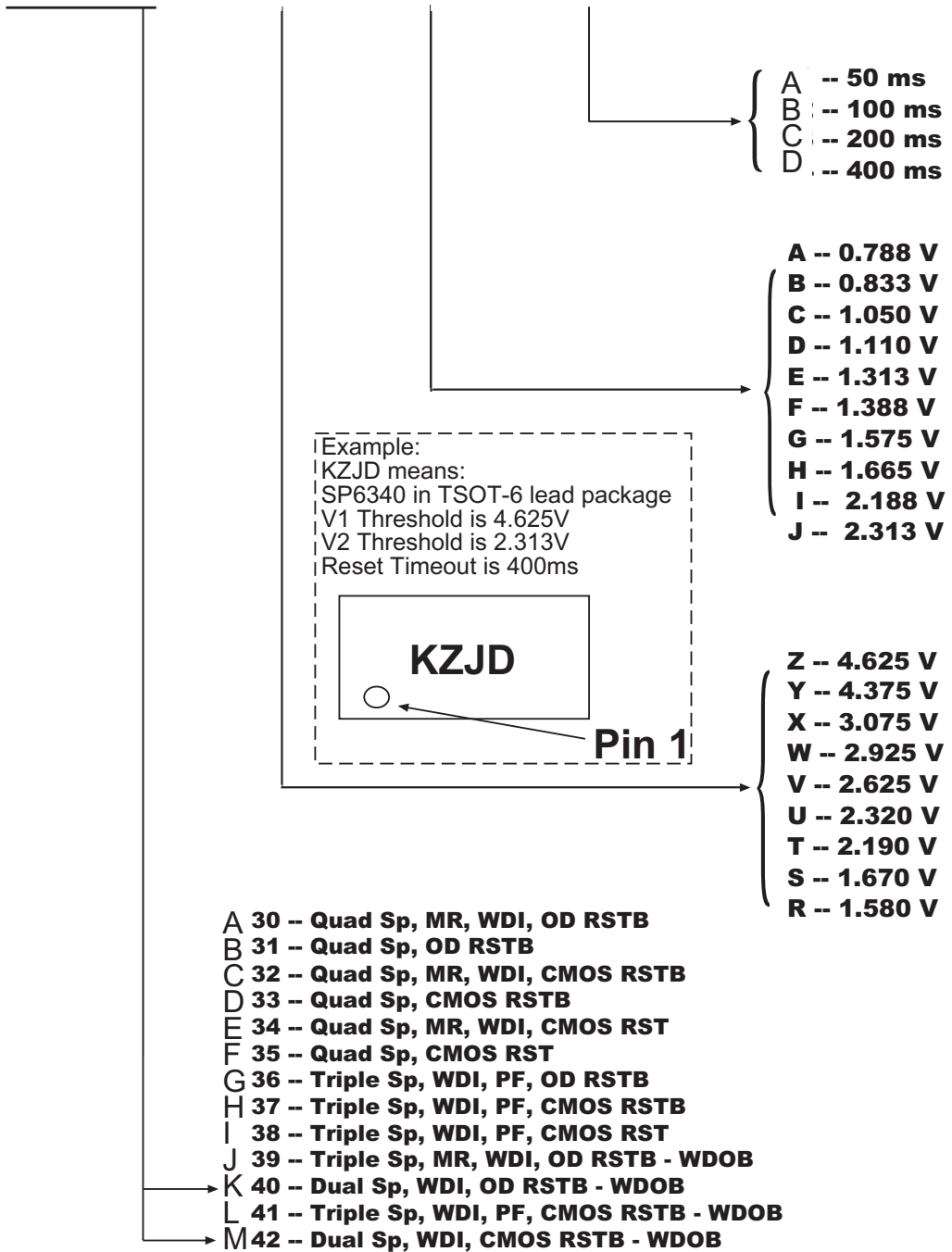
*Reset Good*

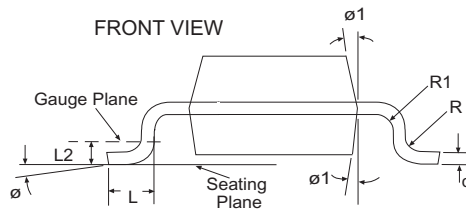
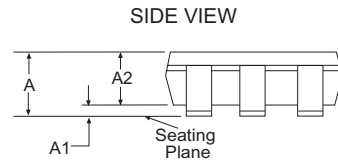
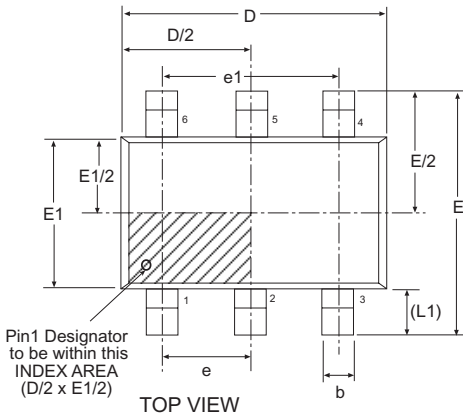


*Reset Timeout vs. Temperature*

# Part Naming Nomenclature

## SP63N - Th1 - Th2 - TOPT





6 Pin TSOT		JEDEC MO-193			Variation AA		
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm			
	MIN	NOM	MAX	MIN	NOM	MAX	
A	-	-	1.10	-	-	0.043	
A1	0.00	-	0.10	0.000	-	0.004	
A2	0.70	0.90	1.00	0.028	0.036	0.039	
c	0.08	-	0.20	0.003	-	0.008	
D	2.90 BSC			0.114 BSC			
E	2.80 BSC			0.110 BSC			
E1	1.60 BSC			0.063 BSC			
L	0.30	0.45	0.60	0.012	0.018	0.024	
L1	0.60 REF			0.024 REF			
L2	0.25 BSC			0.010 BSC			
Ø	0°	4°	8°	0°	4°	8°	
Ø1	4°	10°	12°	4°	10°	12°	
R	0.10	-	-	0.004	-	-	
R1	0.10	-	0.25	0.004	-	0.010	
b	0.30	-	0.50	0.012	-	0.020	
e	0.95 BSC			0.037 BSC			
e1	1.90 BSC			0.075 BSC			
SIPLEX Pkg Signoff Date/Rev:				JL Oct3-05 / Rev A			

## ORDERING INFORMATION

Model	Temperature Range	Package Types
SP6340EK1-L-X-X-X.....	-40°C to +85°C.....	Lead Free 6-Pin TSOT
SP6340EK1-L-X-X-X/TR.....	-40°C to +85°C.....	Lead Free 6-Pin TSOT
SP6342EK1-L-X-X-X.....	-40°C to +85°C.....	Lead Free 6-Pin TSOT
SP6342EK1-L-X-X-X/TR.....	-40°C to +85°C.....	Lead Free 6-Pin TSOT

Available in Lead Free packaging only. /TR = Tape and Reel.

Pack quantity is 2,500 for TSOT-6.

Contact Factory for availability of particular voltage threshold and reset timeout options. Note that the Ordering Information denoting those options corresponds to the Part Naming Nomenclature shown on the previous page.

Ordering example: SP6340EK1-L-W-G-C/TR == W -- 2.925V for Voltage Threshold 1; G -- 1.575V for Voltage Threshold 2; and C -- 200ms reset timeout.



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